Configurable 2 Bits per Cycle Successive Approximation Register for Analog to Digital Converter on FPGA

Lim Yong Hooi, Lo Hai Hiung, Micheal Drieberg and Patrick Sebastian
Department of Electrical and Electronics Engineering,
Universiti Teknologi PETRONAS, 32610, Perak, Malaysia
lo_haihiung@petronas.com.my

***Abstract*—Analog-to-Digital Converter (ADC) technology has been advancing to achieve a balance between speeds, size and cost. Successive approximation register (SAR) ADC is very popular for medium-to-high resolution as it is small but has difficulties in achieving high speed while flash ADC is big and not cost effective. Also, for different purposes, ADC have different resolution requirement. Producing ADCs with different resolution increases cost if it is not used in large scale production. In this paper, we propose to solve the issues of speed, size and cost by presenting a configurable 2 bits per cycle successive approximation register (SAR) ADC for FPGA implementation based on modification from successive approximation method. This SAR utilizes three comparators, instead of one comparator in normal SAR ADC. This enables the SAR to convert 2 bits at a time hence, reducing the conversion time by half, while at the same time, the resolution of this presented SAR is configurable. This increases the reusability of this SAR ADC for various different requirements of resolution. The design is implemented on Altera DE2 board with Cyclone II FPGA at a clock rate of 50MHz and can be boosted to 136MHz. On average, *N* cycles is needed for 2*N* bit resolution.**

Keywords-Successive approximation, binary search, analog, digital, ADC.

I. INTRODUCTION

Following the advancement of CMOS technology that scales down the feature size of CMOS devices, SAR ADCs have gained popularity in medium-to-high resolution application due to lower power consumption and small active area [1]. However, in typical SAR ADC, N steps is needed for resolving N bits resolution ADC, resulting in difficulties to achieve high speed. Asynchronous SAR ADCs are introduced to solve this speed performance issue of SAR ADCs. Similar to conventional SAR ADC, asynchronous SAR ADC is also based on binary search algorithm but instead of one comparator, N comparator are used for an N bit ADC. Output of each comparator becomes the clock for the next comparator while the ADC search from the most significant bit (MSB) to the least significant bit (LSB). Sampling rate of asynchronous ADC is limited by N quantization delays of the comparators and DAC delays since delay in logic feedback path is relaxed [2]. This makes asynchronous SAR ADC capable of achieving high speeds.

Often, different applications require different resolutions of ADC for best speed performance. As ADC are normally designed to have specific resolution of N bits, it is often needed to be redesigned for different applications. This in turn increases the cost if they are not used or needed in large scale or large volume. Hence, configurable resolution is important to increase the reusability of the design. Such configurable resolution is common in flash ADC in order to reduce power consumption by reducing resolution when it is not required [3, 4], though it is not targeting to reduce production cost.

In this work, a configurable resolution binary search ADC that resolves 2 bits at the same time is proposed for FPGA implementation. At each stage, 3 predictions are made and compared by utilizing 3 comparators. This enables 2 bits to be resolved at each state; speeding up N bits ADC from requiring N to N/2 comparison states. At the same time, this work aimed to design an ADC that is reusable for different resolution by allowing resolution configuration in order to reduce production and design cost. The proposed design is implemented on Altera Cyclone II FPGA via Altera DE2 board at a clock rate of 50MHz.

This paper is organized as follows. The Configurable 2 bits per cycle SAR architecture is described in Section II. Section III describes the result of the implementation of the design and compares it with typical SAR ADC. Section IV concludes the paper.

II. CONFIGURABLE 2 BITS PER CYCLE SAR ARCHITECTURE

Conventional flash ADC offers high conversion speed as each conversion is completed in one clock cycle [5-8]. However, flash ADC is exponentially dependence on power and area for resolution and require relatively difficult calibration for many parallel signal paths [9]. In contrast, conventional successive approximation register (SAR) ADC requires only one signal path with one comparator. This makes it possible for SAR to be implemented in a small

area at low power, allowing the architecture to be highly scalable and easier to calibrate [10]. In successive approximation (SA), we rely on a clock to divide the conversion state into equal time slot as the conversion proceeds [11-14]. Therefore, an N bit SAR ADC would at least need N conversion clock cycle to complete the conversion process. In most cases, it needs more than N clock cycles due to the requirement of an initialization before conversion can begin.

In order to increase the speed of conversion, there are two approaches that can be used for SAR ADC: 1) asynchronous processing and 2) more-bit-per-cycle conversion. In asynchronous processing, instead of using synchronous clock, output of each comparator becomes the clock for the next comparator while the ADC search from the MSB to the LSB. Since the delay in the logic feedback path is relaxed, asynchronous processing allows SAR ADC to achieve higher speeds than conventional ones [2]. However, building an asynchronous circuit in FPGA poses a lot of difficulties as timing analysis will fail. Hence, this is not the solution for us since we are looking at designing a SAR ADC that can be implemented on FPGA. In more-bit-per-cycle conversion, SAR ADC is speed up by resolving more bit in a conversion clock cycle. As a tradeoff to resolve more bits in the same clock cycle, it requires more comparators. For a 2-bit-per-cycle SAR ADC, 3 comparators are needed [2, 15]. Going into 3-bit-per-cycle SAR ADC will drastically increase the number of comparators needed from 3 to 7 comparators, increasing the area and power consumption of the ADC. Hence, 2-bit-per-cycle SAR ADC is ideal for its balance between speed, power and area.

Another aim of this design is to reduce the total cost of ADC. This not only can be achieved through increasing speed of conversion while retaining the relatively small size of area needed, but can also be achieved through introducing configurable resolution features in SAR ADC as it increases the reusability of the design. Producing different ADC with each different resolution increases cost if it is not being used in a large scale, by adding reconfigurable resolution capability into SAR, we are able to reduce the time cost and human resource cost in designing and production cost if only small scale of the specific ADC is needed. In short, we intended to design and implement a 2-bit-per-cycle SAR ADC that is customizable and faster for a wider range of application on FPGA.

In this design, SAR ADC is designed to solve two interested bits at a time. 3 comparators are required to simultaneously compare 3 different values in order to solve two interested bits in each clock cycle. The first comparator compares the actual voltage with the generated first hypothetic value with the value 01 is replaced into the two interested bits. The second comparator compares the second hypothetic value 10 is replaced into the two interested bits with the actual voltage. The third comparator's hypothetic value has 11 replaced into the two interested bits. As such, for every cycle, we can solve two bits, speeding up the SAR ADC. Table I shows the truth table of how we deduced the results for the two interested bits. Cases other than these four are not possible. For example, it is impossible for a 2 bit value to be greater than 10 yet smaller than 01.

TABLE I
TRUTH TABLE FOR DEDUCING TWO INTERESTED BITS RESULTS FROM THREE OUTPUTS OF COMPARATORS

Comparator output cases	1st hypothesis (01 is replaced into the interested bits)	2nd hypothesis (10 is replaced into the interested bits)	3rd hypothesis (11 is replaced into the interested bits)	Two bits results deduced from the output of comparators
Case 1	LOW	LOW	LOW	00
Case 2	HIGH	LOW	LOW	01
Case 3	HIGH	HIGH	LOW	10
Case 4	HIGH	HIGH	HIGH	11

*The output of comparator will be logic HIGH if the hypothetical value is greater than or equal to the actual voltage.

Even when ADC is resolving 2 bits per cycle, for 8 bits SAR ADC, it will normally require 5-6 cycles as at least 4 cycles are required to do the conversion for all the 8 bits, one extra cycle for initialization e.g. setting resolution parameter, and another cycle to display valid result before continuing with the next sample. In this work, we minimize it to 4 cycles by combining initialization stage, generating first guess for conversion process and displaying valid data into one single cycle. In another words, the first conversion cycle will cater for setting resolution parameter, displaying previous sample valid result and generating 3 initial guess for comparators. Figure 1 shows the ASM chart of this ADC. The truth table logic is implemented on this control logic where A, B and C is the result of the comparator in logic HIGH or LOW. The decision boxes "count" serves as a check for completion of conversion for all the bits in one sample. T0 is responsible for setting the resolution of the ADC and set the 3 initial guess value to start the process after the start signal is received. Besides, it also serves to display valid conversion result when one whole sample is completed. T1 is responsible to set the two interested bits into 00 and set another 3 new guess value for comparator when the results indicate the interested bits to be 11. T2, T3 and T4 have the similar function as T1 but are activated at different condition, when the results indicate the interested bits to be 01, 10 and 11 respectively.

III. IMPLEMENTATION RESULT ON FPGA AND COMPARISON WITH TYPICAL IMPLEMENTATION

The prototype is designed using Verilog Hardware Description Language with RTL coding style and simulated on Altera Quartus II 9.0. The prototype is also implemented on Altera DE2 Board with Cyclone II EP2C35F672C6 core. The prototype implemented is configurable for its resolution from 4 to 8 bits for testing purposes. A larger range of resolution is achievable by increasing the size of the count register.

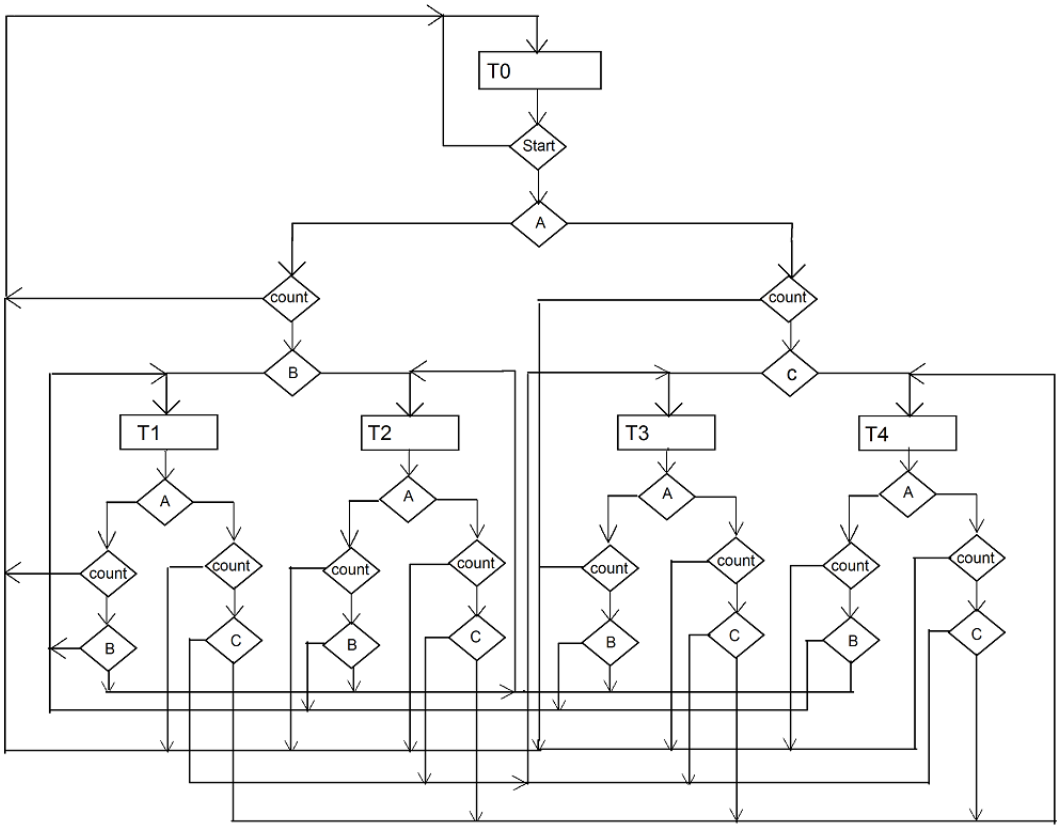

Figure 1. ASM Chart for Configurable 2 Bits per Cycle Successive Approximation Register for Analog to Digital Converter on FPGA

Table II details the FPGA resources utilized for this implementation. Since Altera DE2 board allows maximum clock frequency of 50MHz, this prototype is implemented on a 50MHz clock. However, Quartus 2 simulator has reported that it can be run at a maximum frequency of 190.84MHz (period = 5.240ns) for the implemented configurable 4-to-10 bits SAR for ADC. Since we need N/2 clock cycle to complete the conversion of one sample, for 10 bits SAR, the sampling rate is 38.168MS/s while for 8 bit SAR configuration, the sampling rate is 47.71MS/s. Configured to 6 bits resolution, the prototype register have a sampling rate of 63.613MS/s, while 4 bits resolution configuration gives us sampling rate at 95.42MS/s.

Table III shows a wide range of references work that has been done for ADC with various methods including asynchronous ADC and flash ADC. The table shows clearly that asynchronous ADC and sub flash ADC always perform better than synchronous ADC. However, since we aimed for SAR implementation on FPGA core, both type of the design cannot be implemented. FPGA does not allow asynchronous structure as timing analysis will fail. There are a few works that is similar to our work, especially Casubolo's work which is also a 2 bit per cycle SA ADC [15]. However, in term of sampling rate, the prototype outperforms Casubolo's work which has a sampling rate of 10MS/s for 10 bits

TABLE II
FPGA RESOURCES UTILIZED FOR THE 4-TO-10 BITS CONFIGURABLE RESOLUTION SAR

Family	Cyclone II
Device	EP2C35F672C6
Total logic elements	97 / 33.216 (<1%)
Total combinational functions	91 / 33.216 (<1%)
Dedicated logic registers	50 / 33.216 (<1%)
Total register	50

compared to this prototype which has 38.168MS/s for 10 bits. Besides, Casubolo's design require (N/2)+1 clock cycles for a sample with N bits of resolution while this prototype only requires N/2 clock cycles.

According to Rose [16], even for circuits with logic only, the average FPGA circuit is 3.4 times slower than the application specific integrated circuits (ASIC) implementation. Nevertheless, our prototype shows that even when implemented on FPGA, its sampling rate is still comparable with ASIC structure with 38.168MS/s for 10 bits configurable SAR which is quite near to 10 bits resolution 50MS/s from one of reference SA ADC [17]. Besides, it is even faster than some ASIC ADC design found in [1, 18-20].

TABLE III
COMPARISON OF REFERENCED ADC WORKS

ADC work	Number of resolution bits	Sampling rate (MS/s)	Implementation technology	ADC type
Proposed 4-to-10 bits Prototype SAR	10	38.168	90nm FPGA	Configurable resolution 2 bits per cycle SA
[15]	10	10	MATLAB/SIMULINK	2 bits per cycle SA
[17]	10	50	130nm ASIC	SA
[1]	10	12	130nm ASIC	SA
[3]	8 to 10	150	65nm ASIC	Variable resolution sub flash
Proposed 4-to-10 bits Prototype SAR	8	47.71	90nm FPGA	Configurable resolution 2 bits per cycle SA
[19]	8	0.2	180nm ASIC	SA
[18]	9	50	90nm ASIC	SA
[20]	12	1	600nm ASIC	SA
[2]	6	900	90nm ASIC	Asynchronous binary search
[10]	6	1,000	65nm ASIC	Asynchronous

IV. CONCLUSION

A configurable 2 bits per cycle successive approximation register for ADC on FPGA has been presented and implemented on Altera DE2 FPGA board. This design allows configuration for its resolution and resolve 2 bits per cycle. Configurable resolution makes this design cost effective for reuse in different applications and 2 bits per cycle structure enhances the speed of the ADC. This design is especially suitable as an ADC register core for FPGA.

Future work will focus on improving the speed of this ADC register by using different search algorithms and optimization of the hardware. Future work may also concern the study of the sample/hold circuit synchronization with the FPGA and utilization of op amp as a comparator in this design.

ACKNOWLEDGMENT

The paper is based on research supported by STIRF grant (153AA-D39) from Universiti Teknologi PETRONAS.

REFERENCES

[1] Guan-Ying Huang, C.-C.L., Ying-Zu Lin and Soon-Jyh Chang, *A 10-bit 12-MS/s Successive Approximation ADC with 1.2-pF Input Capacitance*, *IEEE Asian Solid-State Circuits Conference* 2009: Taipei, Taiwan, pp. 157-160.

[2] Ali Mesgarani, S.U.A., *A single channel 6-bit 900MS/s 2-bits per stage asynchronous binary search ADC, 2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS* 2011), page 1-4.

[3] Adimulam, M.K.M., K.K.; Veeramachaneni, S.; Muthukrishnan, N.M.; Srinivas, M.B.; *Low power, variable resolution pipelined analog to Digital converter with sub flash architecture, 2010 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS* 2010), page 204-207.

[4] Adimulam, M.K.V., S.; Muthukrishnan, N.M.; Srinivas, M.B.;, *A Novel, Variable Resolution Flash ADC with Sub Flash Architecture, VLSI (ISVLSI), 2010 IEEE Computer Society Annual Symposium on VLSI (ISVLSI* 2010), page 434-435.

[5] M. Choi and A. A. Abidi, *6b 1.3-GSample/s A/D converter in 0.35um CMOS, IEEE, ISSCC Dig. Tech. Papers* Feb. 2001. p.126-127.

[6] Razavi, B., *Principles of Data Conversion System Design*, in *Wiley-IEEE Press* 1995: New York. p. 114-116.

[7] Geelen, G., *A 6 b 1.1 GSample/s CMOS A/D converter*, in *IEEE ISSCC Dig. Tech. Papers* Feb. 2001. p. 128-129.

[8] Scholtens, P.C.S. *A 2.5 volt 6 bit 600 MS/s flash ADC in 0.25pm CMOS*. in *Proc. ESSCIRC*. Sep. 2000.

[9] G. Van der Plas, S.D., and S. Donnay, *A 0.16 pJ/conversion step 2.5 mW 1.25 GS/S 4b ADC in a 90*

nm digital CMOS process, in *IEEE ISSCC 2006 Digest of. Tech. Papers.* Feb. 2006.

[10] Jing Yang, T.L.N., and Robert W. Brodersen, *A 1 GS/s 6 Bit 6.7 mW Successive Approximation ADC Using Asynchronous Processing.* IEEE JOURNAL OF SOLID-STATE CIRCUITS, AUGUST 2010. **VOL. 45**(NO. 8), page 1469-1478.

[11] Draxelmayr, D., *A 6b 600 MHz 10 mW ADC array in digital 90 nm CMOS*, in *IEEE ISSCC Dig. Tech. Papers*Feb. 2004. p. 264-265.

[12] Liu, C.L.a.B., *A new successive approximation architecture for low-power low-cost CMOS A/D converter.* IEEE J. Solid-State Circuits, Jan. 2003. **vol. 38**(no. 1): p. 54-62.

[13] S. Dondi, D.V., A. Boni, and M. Big, *A 6-bit 1.2 GHz interleaved SAR ADC in 90 nm CMOS*, in *Research in Microelectronics and Electronics*2006. p. 301-304.

[14] J. Sauerbrey, D.S.L., and R. Thewes, *A 0.5 V 1- uW successive approximation ADC.* IEEE J. Solid-State Circuits, Jul. 2003. **vol. 38**(no. 7): p. 1261-1265.

[15] Casubolo, M.G., M.; Lombardi, A.; Maloberti, F.; Malcovati, P.;, *A Two-Bit-per-Cycle Successive-Approximation ADC with Background Offset Calibration*, in *Electronics, Circuits and Systems, 2008. ICECS 2008. 15th IEEE International Conference on* 2008. p. 650-653.

[16] Rose, I.K.J., *Measuring the Gap Between FPGAs and ASICs.* IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, FEBRUARY 2007. **VOL. 26**(NO. 2), p. 203-216.

[17] C. C. Liu, S.J.C., G. Y. Huang and Y. Z. Lin,, *A 0.92mW 10-bit 50-MS/s SAR ADC in 0.13um CMOS process*, in *IEEE Symp. on VLSI Circuits*June 2009. p. 236-237.

[18] Plas, J.G.a.G.V.d., *A 65fJ/conversion-step 0-to-50MS/s 0-to-0.7mW 9b charge-sharing SAR ADC in 90nm digital CMOS*, in *IEEE ISSCC Dig. Tech. Papers*February 2007. p. 246-247.

[19] Lee, H.C.H.a.G.M., *A 65-fJ/conversion-step 0.9-V 200-kS/s rail-to-rail 8-bit successive approximation ADC.* IEEE J. Solid-State Circuits, October 2007. **vol. 42**: p. 2161-2167.

[20] Promitzer, G., *12-bit low-power fully differential switched capacitor noncalibrating successive approximation ADC with 1 MS/s.* IEEE J. Solid-State Circuits, July 2001. **vol. 36**: p. 1138-1143.