Research Article Implementation and Analysis of Biological Synaptogenesis Technique on Nodes and Interconnects for NoC Fault Tolerance

Muhammad Athar Javed Sethi, Fawnizu Azmadi Hussin and Nor Hisham Hamid Department of Electrical and Electronic Engineering, Universiti Teknologi PETRONAS, Tronoh, Perak, Malaysia

Abstract: Bio-inspired Network on Chip (NoC) fault tolerant techniques are a novel way of solving the complex faulty situation in NoC. The excessive and parallel communication requirements of heterogeneous Processing Elements (PE's) in NoC have made the communication structure very complex. The size of the devices are scaled down to support the complexity but the size of interconnects remains the same. Due to this interconnects have contributed to faults. Different fault tolerant techniques have been proposed. But all these conventional algorithms have drawbacks of adaptiveness and robustness. The proposed synaptogensis based bio-inspired technique is based on one of the characteristics of biological brain. This technique is robust as it makes the NoC fault-tolerant and able to reconfigure upon detection of router or interconnect faults. In this study, two techniques based on synaptogensis algorithm have been critically analyzed. In improved algorithm, the packet network latency was reduced to 34.62%, bandwidth was efficiently utilized by 5.03% and throughput was increased by 36.36%. The bio-inspired algorithm has better accepted traffic rate as compared to the traditional fault tolerant technique.

Keywords: Fault tolerant, Network on Chip (NoC), neuron, Processing Elements (PE's), synapse, synaptogenesis

INTRODUCTION

Bio-inspired solutions are playing a vital role in solving the complex and difficult engineering world problems. In order to adopt the biological concept to the engineering world, three things should be considered:

- Identification of engineering concepts which are similar to the nature.
- Whether it is realistic to implement the biological concept.
- How it will be modeled and transformed into the engineering scenario.

The various dynamic characteristics of biological world such as adaptiveness, robustness, learning abilities, effective management of the resources, selforganizing, self-healing and self-optimizing capabilities have always attracted the scientists and researchers to model them in there engineering systems (Dressler and Akan, 2010).

The communication requirements of the devices are increasing day by day as more heterogeneous devices are added on the Network on Chip (NoC) as shown in Fig. 1. Due to parallel and excessive communication between Processing Elements (PEs) and due to the size of interconnects various faults occurs. Permanent and temporary faults are two major types of faults in NoC. The fault tolerance is very important concept nowadays to overcome the temporary faults. Routing algorithms are used to avoid the temporary faults while permanent faults can only be removed by the redundant hardware (Chang *et al.*, 2011; Lehtonen *et al.*, 2010; Koibuchi *et al.*, 2008). To overcome the faults various fault tolerant techniques have been proposed in the literature. They all have the drawbacks.

To overcome the drawbacks of the techniques (Pasricha and Zou, 2011) a biological concept "synaptogenesis" is implement in NoC. This technique has the ability to self-adapt when some neurons get damage in the biological brain. This technique makes the NoC communication fault tolerant and robust.

LITERATURE REVIEW

Deterministic, stochastic, fully adaptive and partial adaptive routing algorithms (Pasricha and Zou, 2011) are four broad categories of routing algorithms.

In deterministic routing the packet routes from the certain point to another using a fixed path. These algorithms lack the adaptiveness but are easy to implement. Xy, yx, xyz and zyx (Pasricha and Zou, 2011; Zhu *et al.*, 2007; Kim and Kim, 2007; Schonwald

Corresponding Author: Muhammad Athar Javed Sethi, Department of Electrical and Electronic Engineering, Universiti Teknologi PETRONAS, Tronoh, Perak, Malaysia

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Fig. 1: Network on chip heterogeneous resources (NI = Network Interface, P = Processor, M = Memory, C = Cache, re = Reconfigurable block)

et al., 2007) are few examples of Dimension Order Routing (DOR) algorithms. DOR algorithms are the simplest algorithm of deterministic routing algorithms. These DOR algorithms are deadlock free.

Directed flooding, N-Random walk and Connection Oriented Stochastic Routing (COSR) are the few types of stochastic routing algorithm. Packet is sent in one or any particular direction depending on the type of algorithm. The advantage of the technique is easy to implement but has drawbacks of congestion, deadlocks, livelocks and high energy and bandwidth consumption (Pasricha and Zou, 2011; Nunez-Yanez *et al.*, 2008; Kim and Kim, 2007).

Routing table is used in fully adaptive routing algorithms to route the packets in NoC. At runtime router decides at which direction packet should be sent to avoid faulty nodes and interconnects. These algorithms are adaptive in nature but the drawbacks are congestion, deadlock situation and high memory requirement for routing table. Source routing for NoC (SRN) and Force Directed Wormhole Routing (FDWR) are two examples among many fully adaptive routing algorithms (Kim and Kim, 2007; Schonwald *et al.*, 2007).

Partial adaptive routing algorithm blocks certain turns in NoC to avoid congestion and deadlock situation. The advantage of this technique is easy to implement. In partial adaptive algorithm there is no routing table due to which these algorithm lacks the adaptiveness. Planar, west first, negative first, north last, south last and odd-even are few examples of planar adaptive routing algorithm (Lehtonen *et al.*, 2010; Pasricha and Zou, 2011; Rantala *et al.*, 2006; Wu, 2000). Details about these algorithms can be found in (Sethi *et al.*, 2013b, 2013a, 2014, 2015).

Due to the drawbacks of the traditional techniques, a novel bio-inspired algorithm "synaptogenesis" is proposed. The bio-inspired algorithm works on the principle of synapse and neuron present in the biological brain.

BIO-INSPIRED NOC METHODOLOGY

The basic building unit of brain is neuron. Biological brain contains around 80 to 120 billion neurons. Two neurons are connected with each other through synapse. Synapse is formed between the axon terminal of one neuron and dendrites of second neuron (Hashmi *et al.*, 2011).

Synaptogensis is the concept of biological brain. It is self-adapt mechanism of biological brain when two neurons want to connect and communicate with each other. In this phenomenon the growth cone present at the top of the axon and dendrites terminal finds the path to the target neuron. The filopodia actually finds the path for connection with the target neuron. Chemical attractant is released by the target neuron to attract the



Fig. 2: Synaptogenesis mechanism (adopted from Rosenzweig *et al.*, 2005)

growth cone. A connection (synapse) is formed between the source and target neuron due to this biological method. This synaptogensis process is shown in Fig. 2 (Rosenzweig *et al.*, 2005).

This biological method is adopted in the bioinspired NoC fault tolerant technique. During the communication between target and source PE, if any interconnect or node becomes faulty a newer synapse will be formed from the neighboring node. This is possible as the target PE and the source PE is constantly communicating with each other. With the help of this method parallel and multiple synapses are constructed between two PE's due to the faulty nodes and interconnect. This multiple synapse utilizes the NoC bandwidth efficiently.

Bio-inspired NoC framework: Heterogeneous Network on Chip simulator (HNOCS), an OMNET++ based simulator (Ben-Itzhak *et al.*, 2012) is used to implement the bio-inspired NoC fault tolerant technique. Two different version of bio-inspired NoC algorithm is implemented. The techniques and results were improved by the implementation of bio-inspired algorithm on the node and later on the interconnect basis.

The bio-inspired NoC technique is working on per link basis. Whenever a faulty node or faulty interconnect is encounter at the scheduler of the port. The scheduler will initiate a new synapse connection from the current node to the destination or will try to connect with the older synapse. The bio-inspired algorithm is robust as it tries to connect with the older synapse and will also avoid the traversal of unnecessary routers. This also decreases the latency of the packets even when faults occur. The bandwidth of the NoC is also efficiently utilized and throughput is slightly decreased for every shorter period of time as the NoC recovers from the faulty node. During the network recovery time the destination will still be receiving the flits from other synapse. These flits have already passed the faulty node.

Bio-inspired NoC Algorithm: At start of the simulation, the nodes at the 4×4 NoC discovers itself. After a network discovery, "synap" signal is initiated by the source PE. The node after receiving the "synap" signal, checks the two hop information from the current node. After receiving the two hops information, the nodes routes the signal to the destination to create a synapse. After the creation of synapse, the source sends the data to the destination over this synapse.

The bio-inspired algorithm increases the efficiency of the network as it only needs one network discovery at the start of simulation. "Synap" signal is able to detect all the static and runtime faults during the simulation.

Information Set (IS) request signal is used by the router to collect the neighbors information. Information Set (IS) requests for the working status of the neighbor node and its neighbor routers information. The neighbor node sends back the information in ISW (west), ISE (east), ISS (south) and ISN (north) response packets. After receiving the information the node decides in which direction it should transfer the packet. The IS packet includes four field having working information (1 = working, 0 = not working, -1 = neighbor doesn't exists) of Direct Neighbor (DN), south, north, west and east neighbor (Nicopoulos *et al.*, 2009).

Temporary synapse connection is initiated by the neighbor node if the interconnect or node becomes faulty during the communication. The flits during the temporary synapse setup will be stored in the node. The temporary synapse builds a new shorter synapse to connect with the older synapse to bypass the faulty node or interconnect. The older synapse continues sending the flits present on it. The connection with the older synapse reduces the latency of the packets and efficiently utilizes the bandwidth as there will be parallel connections (synapses) between source and destinations.

Connection with the older synapse makes the bioinspired algorithm robust as it by pass the faulty region. This phenomenon helps to avoid the unnecessary traversal of the routers. This reduces the network latency of the packets. This temporary mechanism will work for any number of faults in NoC.

The bio-inspired algorithm was modified in two stages. First the algorithm was applied on node basis and later it was modified and tested on interconnect and nodes basis. The algorithm was improved as the various parameters like packet network latency, throughput and bandwidth was efficiently utilized.

Figure 3 shows the case when nodes were made faulty during the simulation. The source (0) initiated a connection to create a synapse with destination (15). The main synapse was broken due to the faulty node of (1) during the simulation. The neighbor nodes detected this faulty node and initiated another shorter synapse to



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Fig. 3: Multiple synapses (cross shows the faulty nodes)



Fig. 4: Multiple connections between source and destination (cross shows that interconnects are faulty)

connect with the older synapse. This reduces the latency of the packets. If the temporary synapse does not find the old synapse on its way, it connects directly with the destination (15). Similarly, when node (11) becomes faulty during the simulation another synapse was created from node 10 to node 15.

The algorithm was update to also handle the interconnect failure along with the node. The results of the bio-inspired algorithm were better than the previous implementation. Figure 4 shows the implementation of bio-inspired algorithm when interconnect failure occurs. The synapse was constructed from source (0) to destination (15) at the start of the communication between them. During simulation the links between various nodes become faulty and a temporary synapse was initiated to bypass the faulty interconnects.

RESULTS

The bio-inspired algorithm was tested in both the cases. The results show that when the bio-inspired algorithm is improved to per link basis, it performed



Fig. 5: Bandwidth vs faults (per node based bio-inspired algorithm)



Fig. 6: Bandwidth vs faults (Improved bio-inspired algorithm)



Fig. 7: Latency vs faults (per node based bio-inspired algorithm)

better. The packet network latency is reduced, throughput is increased and bandwidth is efficiently utilized.

Figure 5 shows the effects of faulty nodes on the bio-inspired algorithm while Fig. 6 shows the results produced by the improved bio-inspired algorithm.

In Fig. 5 and 6 that when there was no faulty nodes and interconnects, the bandwidth utilization of the improved algorithm increased to almost 1989 MBps from 1927 MBps. Similarly, when one fault occurred during the simulation the bandwidth utilization of the improved algorithm is better. The bandwidth utilization is even better when seven interconnects or nodes become faulty.



Fig. 8: Latency vs faults (improved bio-inspired algorithm)



Fig. 9: Packet network latency (per node based bio-inspired algorithm)



Fig. 10: Packet network latency (improved bio-inspired algorithm)

Similarly, the latency of the improved bio-inspired algorithm is reduced. This is shown in Fig. 7 and 8. The latency of the flits in the improved bio-inspired algorithm reduced to almost 49ns from 54ns when three faults were introduced during the simulation.

Figure 9 and 10 shows the packet network latency graphs of the bio-inspired algorithm. The average packet network latency of improved bio-inspired NoC algorithm reduced from 13 ns to 8.5 ns.

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Fig. 11: Throughput (per node based bio-inspired algorithm)



Fig. 12: Throughput (improved bio-inspired algorithm)

Table	1: C	ompar	ison	between	technic	ues

		Parameters (for 16 PE's)						
		Accepted traffic (flits/cycle/node)						
Techniques	Number of faults	0	1	3	5	7		
DBP network (Koibuchi et al., 2008)		0.22	0.18	0.16	0.15	0.14		
Synaptogenesis algorithm		0.39	0.31	0.28	0.26	0.24		

The throughput graphs of Fig. 11 and 12 show that the throughput of the improved bio-inspired algorithm also increases from the previous algorithm. The recovery time from fault is also reduced as can be seen in the Fig. 11 and 12.

The synaptogenesis algorithm has also improved the average throughput and network saturation point (accepted traffic) from the technique mentioned in Koibuchi *et al.* (2008) as shown in Table 1.

CONCLUSION

In this study two synaptogensis base techniques were analyzed. The performance of the NoC is improved with the help of the biological method "Synaptogensis". The bio-inspired algorithm avoided the faulty node and interconnects with the help of shorter and newer synapse. The bio-inspired algorithm improves the bandwidth utilization, throughput and reduces the latency of the packet. In the future, we will further optimize the fault tolerant characteristics of the algorithm and will implement efficient and more robust bio-inspired algorithm.

REFERENCES

Ben-Itzhak, Y., E. Zahavi, I. Cidon and A. Kolodny, 2012. HNOCS: Modular open-source simulator for heterogeneous NoCs. Proceeding of the International Conference on Embedded Computer Systems (SAMOS). Samos, pp: 51-57.

- Chang, Y.C., C.T. Chiu, S.Y. Lin and C.K. Liu, 2011. On the design and analysis of fault tolerant NoC architecture using spare routers. Proceeding of the 16th Asia and South Pacific Design Automation Conference. Yokohama, pp: 431-436.
- Dressler, F. and O.B. Akan, 2010. Bio-inspired networking: From theory to practice. IEEE Commun. Mag., 48(11): 176-183.
- Hashmi, A., H. Berry, O. Temam and M. Lipasti, 2011. Automatic abstraction and fault tolerance in cortical microachitectures. Proceeding of the 38th Annual International Symposium on Computer Architecture (ISCA, 2011). San Jose, CA, pp: 1-10.
- Kim, Y.B. and Y.B. Kim, 2007. Fault tolerant source routing for network-on-chip. Proceeding of the 22nd IEEE International Symposium on Defect and Fault-Tolerance in VLSI Systems (DFT'07). Rome, pp: 12-20.
- Koibuchi, M., H. Matsutani, H. Amano and T.M. Pinkston, 2008. A lightweight fault-tolerant mechanism for network-on-chip. Proceeding of the 2nd ACM/IEEE International Symposium on Networks-on-Chip. Newcastle upon Tyne, pp: 13-22.
- Lehtonen, T., D. Wolpert, P. Liljeberg, J. Plosila and P. Ampadu, 2010. Self-adaptive system for addressing permanent errors in on-chip interconnects. IEEE T. VLSI Syst., 18(4): 527-540.
- Nicopoulos, C., V. Narayanan and C.R. Das, 2009. Network-on-chip architectures: A holistic design exploration. Lecture Notes in Electrical Engineering, Springer, Dordrecht, New York, Vol. 45.
- Nunez-Yanez, J.L., D. Edwards and A.M. Coppola, 2008. Adaptive routing strategies for fault-tolerant on-chip networks in dynamically reconfigurable systems. IET Comput. Digit. Tec., 2(3): 184-198.
- Pasricha, S. and Y. Zou, 2011. A low overhead fault tolerant routing scheme for 3D networks-on-chip. Proceeding of the 12th International Symposium on Quality Electronic Design (ISQED, 2011). Santa Clara, CA, pp: 1-8.

- Rantala, V., T. Lehtonen and J. Plosila, 2006. Network on chip routing algorithms. TUCS Technical Report, No. 779.
- Rosenzweig, M.R., S.M. Breedlove and N.V. Watson, 2005. Biological Psychology: An Introduction to Behavioral and Cognitive Neuroscience. 4th Edn., Sinauer Associates Publisher, Sunderland, Mass.
- Schonwald, T., J. Zimmermann, O. Bringmann and W. Rosenstiel, 2007. Fully adaptive fault-tolerant routing algorithm for network-on-chip architectures. Proceeding of the 10th Euromicro Conference on Digital System Design Architectures, Methods and Tools (DSD, 2007). Lubeck, pp: 527-534.
- Sethi, M.A.J., F.A. Hussin and N.H. Hamid, 2013a. Implementation of biological sprouting algorithm for NoC fault tolerance. Proceeding of the IEEE International Conference on Circuits and Systems (ICCAS, 2013), pp: 39-44.
- Sethi, M.A.J., F.A. Hussin and N.H. Hamid, 2013b. Synaptogenesis based bio-inspired NoC fault tolerant interconnects. Proceeding of the IEEE International Conference on Control System, Computing and Engineering (ICCSCE, 2013), pp: 46-51.
- Sethi, M.A.J., F.A. Hussin and N.H. Hamid, 2014. Bioinspired NoC fault tolerant techniques. Proceeding of the 5th International Conference on, 2014Intelligent and Advanced Systems (ICIAS, 2014), pp: 1-6.
- Sethi, M.A.J., F.A. Hussin and N.H. Hamid, 2015. Survey of network on chip architectures. Parameters, 1: 5-113.
- Wu, J., 2000. A fault-tolerant adaptive and minimal routing approach in n-D meshes. Proceeding of the International Conference on Parallel Processing. Toronto, Ont., pp: 431-438.
- Zhu, H., P.P. Pande and C. Grecu, 2007. Performance evaluation of adaptive routing algorithms for achieving fault tolerance in NoC fabrics. Proceeding of the IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP'2007). Montreal, Que., pp: 42-47.